IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

KIAN TENG ENG ET AL.

Serial No. 09/766,477 (TI-22944.2)

Filed January 19, 2001

For: VERTICAL BALL GRID ARRAY INTEGRATED CIRCUIT PACKAGE

Art Unit 2827

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Jay M. Cantor, Reg. No. 19,906

Sir:

BRIEF ON APPEAL

SPECIAL BASIS

It is believed that this application should be considered on a special basis since it contains withdrawn claims which were copied for purposes of interference.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences though an appeal was filed in the parent application, now Patent No. 6,320,126, and the application was allowed after filing of the Brief on Appeal..

STATUS OF CLAIMS

This is an appeal of claims 21 to 25, 27, 28 and 37, all of the rejected claims. Claims 1 to 20 and 26 have been canceled and claims 29 to 36 and 38 have been withdrawn of which claims 29 to 36 have been copied for purposes of interference more than two years ago. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was not filed after a second or subsequent rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The claimed inventionaccording to claim 21 relates to a process of providing a high density module (200, Figs. 5-7page 26, line 17ff) wherein a circuit board (160, page 27, line 3) having a substantially planar top surface is provided for connection to at least one integrated circuit package (30, 32, page 27 line 1ff) and an integrated circuit package having a pair of opposing major surfaces and at least one edge surface disposed between the opposing major surfaces which is provided with one of the at least one edge surface (92, Figs. 3 and 8, page 25, line 19) having at least one electrical terminal (100, Figs. 4-8, page 26, lines 8 and 15) disposed thereon. The at least one electrical terminal on the at least one edge surface of the integrated

circuit package is electrically connected to the top surface (170, Fig. 8, page 28, line 5) of the printed circuit board at an acute angle (Figs. 7, 8A and 8B, page 28, line 9ff, page) with the top surface of the printed circuit board. A solder ball (150, page 28, line 17) can be disposed between the side surface terminal of the integrated circuit package and the top of the circuit board. The acute angle is preferably between 30 and less than 90 degrees to the circuit board.

GROUNDS OF REJECTION

Claims 21 to 25 and 28 were rejected under 35 U.S.C. 102(b) as being anticipated by Cotues et al. (U.S. 5,239,447).

Claims 27 and 37 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cotues et al.

Claims 21 to 25, 27, 28 and 37 were rejected as being unpatentable over Suzuki et al. (U.S. 5,726,492) in combination with Fujisawa et al. (U.S. 6,094,356).

ARGUMENT

Claims 21, 22, 24, 25 and 28 were rejected under 35 U.S.C. 102(b) as being anticipated by Cotues et al. (U>S. 5,239,447). The rejection is without merit.

Claim 21, from which claims 22, 24, 25 and 28 depend, requires, among other features, "electrically connecting said at least one electrical *terminal on said at least one edge surface of said integrated circuit package* to said top surface of said printed circuit board at an acute angle with said top surface of said printed circuit board". No such feature is taught or even remotely suggested by Cotues et al. Note with respect to figures 4 and 5 of Cotues et al. that the terminal is not on the edge surface of the package but rather on a major surface. The surface 76 of Cotues et al. is specifically stated at column 5, lines 47ff to be "a dielectric layer such as a silicon

dioxide layer or other dielectric coating on a silicon electronic device 40'. It follow that the edge surface of the integrated circuit package of Cotues et al. is not an electrical terminal as required by claim 21 and is not electrically connected to the circuit board and, accordingly, a rejection under section 102 fails to meet the statutory requirements..

Claims 22 to 25, 27 and 28 depend form claim 21 and therefore define patentably over Cotues et al. for at least the reason ns set forth above with reference to claim 21.

In addition, claim 22 further limits claim 21 by requiring the step of electrically and perpendicularly connecting at least two integrated circuit packages to the circuit board. No such combination is taught or suggested by Cotues et al.

Claim 25 further limits claim 21 by requiring the step of integrally attaching at least three tabs to said circuit board. No such combination is taught or suggested by Cotues et al.

[Claim 23 further limits claim 21 by requiring the step of disposing a solder ball between the side surface terminal of the integrated circuit package and the top of the circuit board. No such combination is taught or suggested by Cotues et al.]

Claim 25 further limits claim 21 by requiring the step of integrally attaching at least three tabs to said circuit board. No such combination is taught or suggested by Cotues et al.

Claim 28 further limits claim 21 by requiring that the at least one edge surface is four edge surfaces, each of the four edge surfaces disposed between the major surfaces to form a closed package with the major surfaces. No such combination is taught or suggested by Cotues et al.

Claims 27 and 37 were rejected under 35 U.S.C. 103(a) as being unpatentable over Cotues et al. The rejection is without merit.

Claim 27 further limits claim 21 by requiring that the integrated circuit package be further defined as being connected at an acute angle between 30 and less than 90 degrees to the circuit board. No such feature is is taught or suggested by Cotues et al. either alone or in the combination as claimed.

Claim 37 is patterned after claim 27 and defines patentably over Cotues et al. for the reasons presented above with reference to claim 27.

Claims 21 to 25, 27, 28 and 37 were rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U.S. 5,726,492) in combination with Fujisawa et al. (U.S. 6,094,356). The rejection is without merit.

All of the rejected claims other than claim 37 depend from claim 21 and claim 37 is patterned after claim 27. Accordingly, the argument presented hereinbelow applies to all of these rejected claims.

It is readily apparent that Suzuki et al. teach mounting semiconductor chips 22 onto a substrate 24 with wiring pattern thereon 24a via solder bumps 23a. It is not the chip 22, but rather the substrate 24 via the wiring pattern 24a thereon which is connected to the main substrate 32. This has nothing whatsoever to do with the claimed invention herein. It therefore follows that, even were Fujisawa et al. to teach that which is alleged, there would still be no basis for the combination. However, a review of Fujisawa et al. will indicate that the terminal 16A is not connected to the edge surface of the chip 12, but rather travels over a major surface thereof where the connection is made. It follows that the terms of the rejected claims are not met by either reference or any combination thereof, proper or improper. Furthermore, it is readily apparent that the structure of Fujisawa et al. would require several additional steps in comparison with the subject invention to provide the connection since it would require the formation of

terminal 28A on the chip 12, the formation of the solder member 32, the and the affixing of the lead 16A to the terminal 28A and the solder member 32, this requiring far more steps than merely forming a terminal on the end of the chip and affixing it to the printed circuit board as claimed.

With reference to the allegation that the claims do not require that "the terminal (48) is electrically connected to a package's edge between two major surfaces" reference is invited to figures 7, 8A and 8B and to claim 21 where it is specifically stated "providing an integrated circuit package having a pair of opposing major surfaces and at least one edge surface disposed between said opposing major surfaces, one of said at least one edge surface having at least one electrical terminal disposed thereon; and electrically connecting said at least one electrical terminal on said at least one edge surface of said integrated circuit package to said top surface of said printed circuit board at an acute angle with said top surface of said printed circuit board". The edge surface is not, by definition, a major surface.

Claims 29 to 36 are not a part of this appeal, but are included hereinbelow for the benefit of the Board since they were copied for purposes of interference and should be addressed in this application at some point in the prosecution under the present Rules.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

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CLAIMS APPENDIX

The claims on appeal read as follows:

Claim 21 A process of providing a high density module produced by a process comprising the steps of:

providing a circuit board having a substantially planar top surface for connection to at least one integrated circuit package;

providing an integrated circuit package having a pair of opposing major surfaces and at least one edge surface disposed between said opposing major surfaces, one of said at least one edge surface having at least one electrical terminal disposed thereon; and

electrically connecting said at least one electrical terminal on said at least one edge surface of said integrated circuit package to said top surface of said printed circuit board at an acute angle with said top surface of said printed circuit board.

Claim 22 The process as recited in claim 21 further including the step of electrically connecting at least two said integrated circuit packages to said circuit board at a said edge.

Claim 23 The process as recited in claim 21 further including the step of disposing a solder ball between said side surface terminal of said integrated circuit package and said top of said circuit board.

Claim 24 The process as recited in claim 21 further including the step of disposing solder columns between said integrated circuit and said top of said circuit board.

Claim 25 The process as recited in claim 21 further including the step of integrally attaching at least three tabs to said circuit board.

Claim 27 The process as recited in claim 21 wherein said integrated circuit package is further defined as being connected at an acute angle between 30 and less than 90 degrees to said circuit board.

Claim 28 The process as recited in claim 21 wherein said at least one edge surface is four edge surfaces, each of said four edge surfaces disposed between said major surfaces to form a closed package with said major surfaces.

Claim 29. A microelectronic package comprising:

a first microelectronic substrate;

a second microelectronic substrate that is oriented at an acute angle relative to the first microelectronic substrate; and

a plurality of solder bumps between the first and second microelectronic substrates, adjacent an edge of the second microelectronic substrate, that directly connect the second microelectronic substrate to the first microelectronic substrate and that are confined to within the edge of the second microelectronic substrate.

30. A microelectronic package according to claim 29 wherein the acute angle includes a vertex and wherein the edge of the second microelectronic substrate is adjacent the vertex.

31. A microelectronic package according to claim 29 wherein the plurality of solder bumps is a plurality of first solder, the microelectronic package further comprising:

a third microelectronic substrate on the first microelectronic substrate that laterally overlaps the second microelectronic substrate; and

a plurality of solder bumps that directly connect the third microelectronic substrate to the first microelectronic substrate.

32. A microelectronic package according to claim 31 wherein the second and third microelectronic substrates are oriented parallel to one another at the acute angle relative to the first microelectronic substrate.

33. A microelectronic package according to claim 32 wherein the plurality of second solder bumps are between the first and third microelectronic substrates, adjacent an edge of the third microelectronic substrate and are confined to within the edge of the third microelectronic substrate.

34. A microelectronic package according to claim 33 wherein the acute angle includes a vertex and wherein the edge of the third microelectronic substrate is adjacent the vertex.

35. A microelectronic package according to claim 31 wherein the third microelectronic substrate extends between the first and second microelectronic substrates.

36. A microelectronic packaging method comprising:

orienting a second microelectronic substrate at an acute angle relative to a first microelectronic substrate such that a plurality of solder bumps extend between the first and second microelectronic substrates, adjacent an edge of the second microelectronic substrate; and

reflowing the plurality of solder bumps to connect the second microelectronic substrate to the first microelectronic substrate while confining the plurality of solder bumps to with the edge of the second microelectronic substrate during reflowing.

Claim 37 A process of providing a high density module produced by a process comprising the steps of:

providing a circuit board having a substantially planar top surface for connection to at least one integrated circuit package;

providing an integrated circuit package having a pair of opposing major surfaces and at least one edge surface disposed between said opposing major surfaces, one of said at least one edge surface having at least one electrical terminal disposed thereon; and

electrically connecting said at least one electrical terminal on said at least one edge surface of said integrated circuit package to said top surface of said printed circuit board at an acute angle between 30 and less than 90 degrees with said top surface of said printed circuit board.

Claim 38 A high density module comprising:

a circuit board having a substantially planar top surface for connection to at least one integrated circuit package; and

an integrated circuit package having a pair of opposing major surfaces and at least one edge surface disposed between said opposing major surfaces, one of said at least one edge surface having at least one electrical terminal disposed thereon;

said at least one electrical terminal on said at least one edge surface of said integrated circuit package electrically connected to said top surface of said printed circuit board at an acute angle between 30 and less than 90 degrees with said top surface of said printed circuit board.

EVIDENCE APPENDIX

Not applicable

RELATED PROCEEDINGS APPENDIX

Not applicable